OIPE JC25
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PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Sarpeshkar et al.	**GROUP:**	Unknown
SERIAL NO:	10/625,360	**EXAMINER:**	Unknown
FILED:	07/23/2003		
FOR:	SYSTEM AND METHOD FOR DISTRIBUTED GAIN CONTROL		

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INFORMATION DISCLOSURE STATEMENT

In compliance with 37 C.F.R. §§1.56, 1.97, and 1.98, Applicant submits copies of the documents listed on the attached Form PTO-1449.

The listed documents were recently cited in a corresponding PCT application, and a copy of the International Search Report is being submitted herewith for purposes of convenience.

The Commissioner is authorized to charge Deposit Order Account No. 19-0079 for any further fee that is required.

Respectfully submitted,

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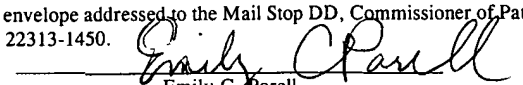
I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the Mail Stop DD, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



Emily C. Porell

02/11/2004
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FORM PTO-1449 (Rev. 5/92) SAMUELS, GAUTHIER & STEVENS 225 Franklin Street, Boston, MA 02110 Telephone: (617) 426-9180 **INFORMATION DISCLOSURE STATEMENT BY APPLICANT**	ATTORNEY DOCKET NO. MIT.8924 APPLICANT Sarpeshkar et al. FILING DATE July 23, 2003	SERIAL NO. 10/625,360 GROUP EXAMINER Unknown

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO
	AE						

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL		
	AF	"Design of an Analogue VLSI Model of an Active Cochlea," Fragniere et al. *Analog Integrated Circuits and Signal Processing*. May-June 1997. Kluwer Academic Publishers, Netherlands. Vol. 13, No. 1-2.
	AG	"Silicon Cochlea and its adaptation to spatial localization," Grech et al. *IEE Proc.-Circuits Devices Syst.* April 1999. Vol. 146, No. 2.
	AH	"ASIC Implementation of the Lyon Cochlea Model," Summerfield et al. *Digital Signal Processing 2, Estimation, VSLI.* San Francisco, CA. March 1992.
	AI	"A Low-Power Wide Dynamic-Range Analog VLSI Cochlea," Sarpehskar et al. Analog Integrated Circuits and Signal Publishing. 1998. Kluwer Academic Publishers, Boston, MA.
	AJ	"Energy-Efficient Adaptive Signal Decomposition: The Silicon and Biological Cochlea," Rahul Sarpeshkar. *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems*. May-June 1999. Orlando, Florida.
	AK	"A Computational Cochlear Nonlinear Preprocessing Model with Adaptive Q Circuits," Hirahara et al. *ICASSP*, 1989. P. 496-499.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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